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REVIEW-ANALYSIS OF EXISTING TYPES OF ADCs WITH THEIR SUBSEQUENT SELECTION FOR USE IN FINE SUBSTANCE OBTAINING SYSTEMS

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Abstract. *The paper draws attention to the issue of global climate change on the planet. This process is influenced by the burning of natural resources. Thus, nanotechnology is seen as a possible solution to this issue. The term "nanotechnology" is considered in the perspective of commencing and applying novel materials, devices and systems. Their structure is varied and managed in nanometer range down to atoms, molecules and supramolecular formations. It is shown that the number of atoms in the bulk elements of such structures becomes close to A number of atoms on the surface of these elements. Due to the high surface energy, nanostructures are extremely active, interact with outer sources, changing properties of both environment and their own. The role of the fine substances in the nanostructure development is shown.*

In addition, the role of analog-to-digital converters in the design of systems for the deep purification of substances is also presented.

The schematic diagrams of ADC with two-cycle integration are shown. The full cycle of its operation consists of two clock cycles. In the first clock cycle, the input voltage is integrated over a fixed time interval using an analog integrator.

In the second cycle, the capacitor is discharged from the reference voltage source, which has the opposite polarity to the input voltage and is connected to the integrator. This process continues until the condenser returns to its initial condition.
The operation of ADC with successive approximation is described in detail. Methods of increasing the speed of ADC with successive approximation and the possibility of simplifying the circuit for designing this type of ADC are also considered.
Parallel ADCs with direct logical convert are considered, while it is indicated that this type of coding logic uses a direct transition from the unitary code that takes place at the output of the comparators.

In addition, the operation oftracking type ADC based on the feedback voltage of the ADC output code is considered. The components of errors introduced both by the elements of the structure and the errors appearing in the process of transformation are shown.

For devices designed to determine the –inception‖ and –end‖ points of the peak, the type of an ADC was selected that could be used in systems for deep purification of substances.

Keywords: *nanotechnology, nanostructures, analog-to-digital converter, a digital-to-analog converter, highly pure substances, the system for deep purification of substances, noise immunity, the error of analog-to-digital conversion.*

INTRODUCTION. Recently, there has been a global climate change on Earth. All this is due to the increase in the atmosphere of the gas CO_2. This gas is generated mainly by burning natural energy resources such as natural gas, oil, and coal. To solve this problem, it is necessary to expand the scope of the development of energy-saving technologies and at the same time pay special attention to the development trends of nanotechnology.

The term "nanotechnology" is understood as the creation and use of materials, devices, and systems, the structure of which is regulated on a manometer scale at the level of the sizes of atoms, molecules, and submolecular formations. The number of atoms in the volumes of elements of such structures becomes close to the number of atoms on the surface of these elements. The consequence of this is a change in the properties of elements depending on their size. The reason for this is that the dimensions of the nanostructure are commensurate with or less than the characteristic scales of physical phenomena included in the description of a property or process (wavelength of oscillations, the magnitude of the magnetic domain, mean free path of an electron, etc.)

Due to the high surface energy, nanostructures are extremely active, interact with the environment, changing the properties of both their own and the environment.

Recent studies clearly indicate the important role of nanostructures in various fields of science and technology. Carbon nanotubes have shown outstanding strength properties, nanoparticles - the ability to selectively penetrate cancer cells, etc. they have unique physical, chemical, and biological properties.

Recent studies clearly indicate the important role of nanostructures in various fields of science and technology. Carbon nanotubes have shown outstanding strength properties, nanoparticles - the ability to selectively penetrate cancer cells, etc. they have unique physical, chemical, and biological properties.

Obtaining highly pure substances with the presence of impurities less than 10^{-8} % is possible using a multi-column adsorption system for cleaning chemical elements. The number of columns varies from 500 to 10,000 in the purification system. When obtaining high-purity substances in large quantities, an adsorption system with at least 5000 columns should be used.

When constructing a system for deep purification of substances, one should have the same number of amplifiers, analog-to-digital converters, and devices for determining the beginning and end of a peak, as the number of absorption columns in the system for deep purification of substances. This work is devoted to a review of the existing types of ADCs with the subsequent selection of ADCs for use in systems for obtaining highly pure substances.

MATERIAL AND METHODS. One of the most common converters is an ADC with push-pull integration. The full cycle of its work consists of two tacts. In the first, with the help of an analog integrator, the input voltage is integrated over a fixed time interval $T = N_{\max}\Delta t_c$, where $N_{\max}$ is the counter capacity, which determines the resolution of the ADC. As a result of this, a charge accumulates on the integrating capacitor

$$q_1 = \frac{\overline{U}_{in}T}{RC}, \qquad (1)$$

where $\overline{U}_{in}$ is the average value of the input voltage over time *T*.

In the second cycle, the capacitor is discharged from the reference voltage source U_{ref}, which has a polarity opposite to the input voltage and is connected to the integrator using the switch *Kl*. This process continues until the capacitor returns to the initial conditions (Fig. 1), which is fixed by the comparator. As a result, the charge removed from the capacitor

$$q_2 = \frac{U_{ref}t}{RC}, \qquad (2)$$

where *t* is the capacitor discharge time. This time is variable, and its subsequent measurement by means of counting pulses with a repetition period Δt_c allows obtaining a digital equivalent of $\overline{U}_{in}$.

First, the integration of the input signal leads to its averaging and smoothing of all interference, interference, and noise, which are fast compared to the integration time. As shown, integrating the signal over time *T* is equivalent to filtering it with a low-pass filter having a frequency response.

This characteristic allows you to determine the degree of suppression of various frequency components present at the input of the integrator, if the value of t_c is replaced by *T*. In particular, it is easy to see that if you choose the integration interval *T* as a multiple of the period of the mains frequency, for example, 50 Hz, then at this frequency the pickups passing through the power circuits and being one of the factors limiting the accuracy of the ADC will be completely suppressed.

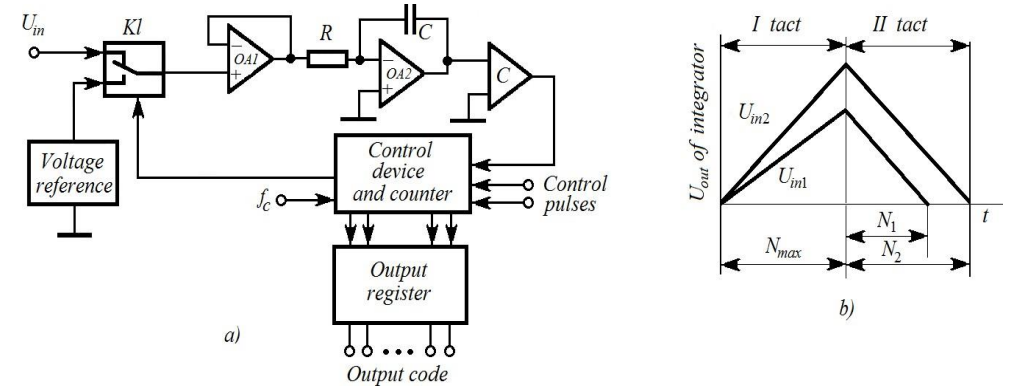

Figure 1. Block diagram of an ADC with push-pull integration (a) and timing diagrams explaining its operation (b).

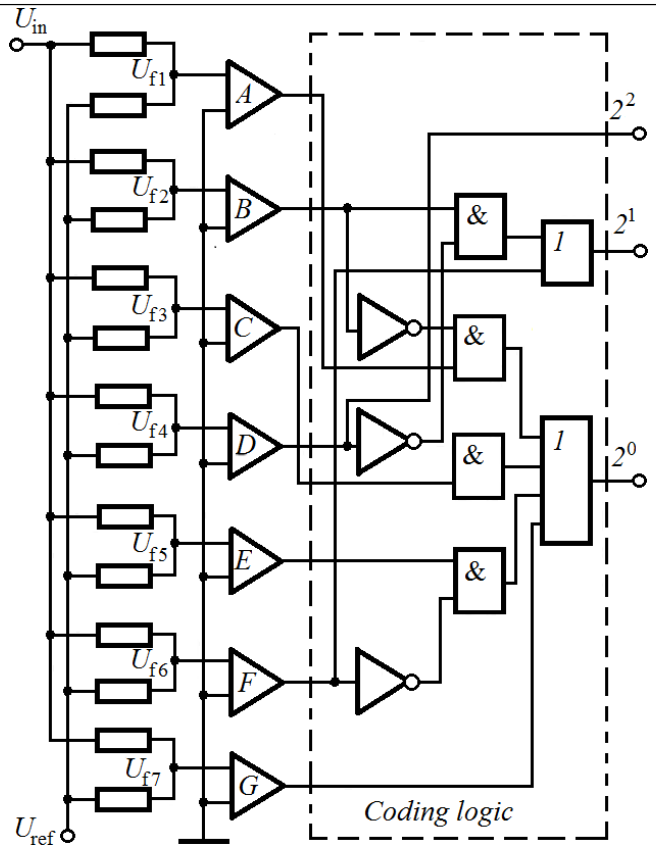

Figure 2. Diagram of a parallel ADC with a direct transition from unitary code to binary

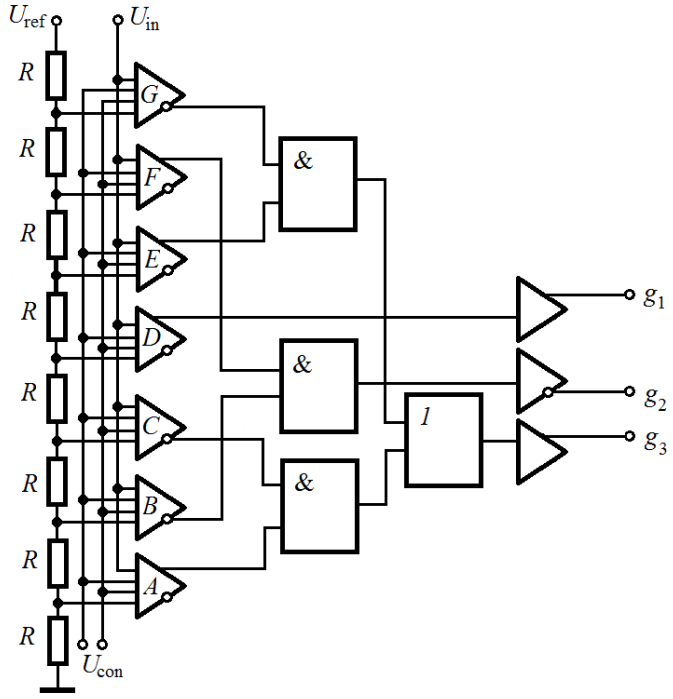

Figure 3. Block diagram of a 3-bit parallel ADC operating in Gray code.

In terms of the theory of signal processing, what has been said can be interpreted as an increase in the ratio of the signal to noise at the output of the integrator, and since this ratio is a criterion for noise immunity, this result means an increase inthe noise immunity of ADCs using input signal integration.

Second, the integration of the input signal leads to a decrease in the dynamic errors of the ADC associated with the change in the signal during the conversion. In particular, the components of the dynamic error, caused by the odd derivatives of the input signal, disappear.

Third, the use of push-pull integration makes it possible to compensate for several components of the static error and significantly increase the overall conversion accuracy. These components include errors in the buffer amplifier arising from a change in the gain of the common-mode signal, errors in the integrator due to a change in the integrator's time constant, and drifts of these components if their speed is such that they can be neglected during one conversion. The total time of one conversion of an *m*-bit ADC of successive approximations consists mainly of the time required to carry out *m* successive approximations, therefore, the correct choice of the time of one approximation (iteration) is the main moment that determines the speed of such ADCs.

Here, the individual components have the same meaning as the expression (delays in switching on digital circuits are deliberately not taken into account here due to their smallness). In the ADC, the maximum input signal is 4 V. The maximum settling times of the DAC and OA at large input voltages of the order of $U_{\text{in max}}/2$, which occur at the first iteration, are 0.3 and 1.5 μs, respectively. As follows from the examples considered earlier, in order for the comparator not to introduce significant additional noise, it must have a sensitivity of at least 0.1 ... 0.2 quantization step, which corresponds to this ADC. It should be noted that with a decrease in voltage drops acting at the input of the op-amp, its settling time with the same error decreases to 0.5 1.0 μs. This allows you to fundamentally reduce the total conversion time of the ADC under consideration, for example, to 10 μs, if you reduce the duration of the second and subsequent iterations, accordingly changing the frequency of the pulse generators.

Let's consider a circuit of a more accurate and perfect successive approximation ADC built based on a 12-bit DAC.

One of the features of its operation is the use of a comparator in the current comparison mode, while in the example considered, the comparator compared voltages.

As shown, the main output parameter of most microelectronic DACs is current, the value of which is proportional to the code supplied to it. In cases where an output voltage is required for subsequent use, a summing operational amplifier is turned on, which simultaneously converts the current into a voltage. However, this additional operation increases the settling time of the output voltage with a given error. This is exactly what happened in the previous example, when, due to the presence of an operational amplifier, it was necessary to choose a time of one iteration of 2 μs, although the DAC itself allows you to work much faster. And in the considered DAC, the settling time of the output current with an error of the order of 0.5 quantization step is of the order of 300 ns. Therefore, the rejection of the operational amplifier in this ADC is caused by the desire to increase its performance.

When using the comparator in the current comparison mode, its inverting input is grounded, and the input signal through the resistor R_{in} is fed to the non-inverting input together with the DAC output current I_{DAC}. The comparator essentially reacts to the sign of the difference in currents $\Delta I = I_{\text{in}} - I_{\text{DAC}}$, where I_{in} is the current through the resistor R_{in} created by the positive input voltage. To limit the voltage swing at the comparator input and increase its slew rate in this mode, a two-sided diode limiter is used, similar to that used in voltage comparators. In order not to decrease the speed of the comparator, these diodes must be fast and not have the effect of accumulating minority carriers. Schottky diodes meet these requirements best of all.

The advent of integrated DACs made in the same package together with a reference voltage source, integrated circuits of the successive approximation register, as well as several

integrated voltage comparators makes it possible to design successive approximation ADCs based on only three integrated circuits.

You can increase the speed of serial ADCs and somewhat simplify their circuit if you abandon the software control method and switch to asynchronous logic. A common feature of constructing an ADC with constant thresholds with a binary code is the sequential inclusion of identical stages, each of which consists of an amplifier with two discretely controlled values of the transmission coefficients and a comparator that switches these coefficients. Therefore, such converters are usually called cascades.

The input signal goes to the high-order comparator. Its threshold voltage $U_{th1} = U_{in\ max}$/ [2]. If $U_{in} > U_{th1}$, then the comparator is triggered and turns on the transistor T_2 of the current switch T_1, T_2. It's so that the voltage drop across it was equal to $U_{in\ max} / 2$.

As a result, there is a residual voltage at the output of the composite emitter follower:

$$U_{out1} = U_{in2} = U_n - \frac{U_{inmax}}{2} \qquad (3)$$

when$U_{in} < U_{f1}$, the input signal completely passes through the composite follower and enters the input of the comparator and the follower, which form the second stage. For it, $U_{f2} = U_{inmax} / 4$, $R_2 = R_1 / 2$, which ensures, with the same collector current of the key, a voltage drop across it equal to $U_{inmax} / 4$.

The third stage, which forms the least significant bit of the output code, consists of a comparator, the threshold voltage of which is equal to EMP.

The use of emitter followers and current switches in conjunction with such high-speed comparators, such as, for example, an integral comparator Am685 with ESL outputs, makes it possible to obtain the response time of one stage of 10 ... 15 ns. However, such a speed can be realized only when the number of converter bits is not more than 3 4. Otherwise, the settling time of one stage with an acceptable error will increase, and the speed of the ADC will decrease, as is the case for the successive approximation ADC.

Forward Convolution Parallel ADCs This type of coding logic uses a direct transition from a unitary code that occurs at the output of the comparators to a binary code. The ADC in Figure 2.comparators with one output is used. The formation of the least significant bit can be described by the Boolean equation:

$$\alpha_3 = \overline{AB} + \overline{CD} + E\overline{F} + G \qquad (4)$$

where symbols with a dash and without a dash mean direct and inverted (using three inverters) outputs of the corresponding comparators. The formation of the second and first digits corresponds to the equations:

$$\alpha_2 = B\overline{D} + F \quad (5)$$

$$\alpha_1 = D$$

One of the most effective ways to deal with unwanted failures during transitions of the output code, for example, from 011 to 100, is the use of coding logic that works in the Gray code.

The circuit (Fig. 3) uses gated comparators with memory in the form of a trigger-latch, similar, for example, to the Am685 comparator, which has both direct and inverse outputs. The least significant bit is formed according to the boolean expression:

$$g_3 = A\overline{C} + E\overline{G} \ , \qquad (6)$$

Consider the operation of a tracking type ADC. When the input voltage and the feedback voltage are equal, the ADC output code fluctuates around the middle position with an accuracy of one least significant bit, as is the case in any discrete tracking system.If in this state of dynamic equilibrium the input signal starts to change, then the output code of the converter will track it with an error equal to one of the least significant bit, if the condition is met.

This ratio determines the aperture error of the tracking ADC, and the period of the counting pulses Δt_c is its aperture time. Thus, the period of the counting pulses, characterizing the speed, must be selected based, on the one hand, from the permissible value of the aperture

error for a given input signal, and on the other hand, from ensuring the operation of all digital devices, a comparator for establishing transient processes at the DAC output with an error, constituting a certain part of the unit of the least significant bit, as is the case in an ADC with a step sawtooth voltage.

For simplicity, the analog voltage comparator and DAC, including the output operational amplifier and the voltage reference, can be considered the main sources of a static error. The method for calculating the static error of a DAC and its main components can be fully applied to a tracking type ADC. Let us consider in more detail the components of the error introduced by the comparator.

The comparator plays an important role in the operation of such ADCs, controlling the operation of the downward counter and determining the clarity of the transition lines from one code value to another. It is easy to see that comparators having a static characteristic can easily be excited in the vicinity of the threshold zone, even in the presence of slight interference. As a result, the output codes of the transformer can change dramatically when transitioning from one value to another. Therefore, for the ADCs under consideration, it is recommended to use comparators with adjustable hysteresis with a static characteristic. Although hysteresis leads to the appearance of an additional conversion error, it eliminates false alarms and the possible generation of a comparator in the vicinity of the threshold zone.Suppose that there are no components of the DAC error in the ADC quantization characteristic, and all deviations of the real characteristics from the ideal one are caused by such comparator parameters as hysteresis and uncertainty zone. The first component leads to some constant displacements of the transition lines by $\pm\ \upsilon_{\text{h}}$, and the second - to blurring these lines with a standard deviation σ_{d}. Considering these values constant for the entire quantization characteristic and applying to the last formula, we have for the power of the quantization noise $P_{\text{n}} = h^2/12 + v_h^2 + \sigma_{\text{d}}^2$.

RESULTS. It should be noted that when constructing devices for determining the beginning and end of a peak based on standard ADC types, the following methodology is used. Two values U_1 and U_2 are stored at the ADC output with a time interval Δt. When determining the beginning of the peak, the increment of the input signal over time Δt is determined. This increment is expressed as ΔU.

$$\Delta U = U_2 - U_1 (7)$$

The moment of fulfillment of inequality (8) is taken as the beginning of the peak t_{beg}.

$$\Delta U \geq U_{\text{thr}} \ (8)$$

where$U_{\text{thr}}$is a certain threshold value of exceeding which is taken as the beginning of the peak.

When determining the end of the peak, the decrease in the input signal is measured over the time Δt. This value is expressed as ΔU.

$$\Delta U = U_1 - U_2 \ (9)$$

The moment of fulfillment of inequality (10) is taken as the end of the peak t_{end} .

$$\Delta U \leq U_{\text{thr}} \ (10)$$

whereU_{thr} is a certain threshold value, the decrease of which is taken as the end of the peak.

Now let's consider an approximate hardware solution for this presentation. To store the values of $U_1$and U_2, twelve-bit registers, comparison circuits, a sensor, and a clock generator can be used. Taken together, this turns out to be a rather complex device. When constructing devices for determining the beginning and end of a peak based on a tracking ADC, another technique can be used. That is, based on the tracking ADC, it becomes possible to build these devices based on the signals at the information inputs "+1" and "-1" of the reverse counter included in the tracking ADC.

It should be noted that when the control signal is set at the information input "+1" of the reverse counter, the output signal at the output of the tracking type ADC will increase continuously. While when the control signal is set at the information input "-1", the output signal at the ADC output will go downward.Consider the hardware component of a device for determining the beginning and end of a peak based on a tracking ADC. It will consist of a four-bit shift register and a logical element "4&" at the output of which a signal corresponding to the beginning and end of the peak will appear.

CONCLUSION. As can be seen from the above, the devices for determining the beginning and end of the peak built based on a tracking type ADC are an order of magnitude simpler and cheaper than similar devices based on other types of ADCs. It should be noted that the ADC and the device for determining the beginning and end of the peak are connected to each adsorption column individually. As a result, when building a system for deep purification of substances, ten thousand pieces of ADC and devices for determining the beginning and end of the peak should be used.Hence it follows that when using a tracking type ADC, it becomes possible to obtain very large cost savings when creating a deep cleaning system.Based on the above, when building a system for the deep cleaning of substances, one should choose an ADC of the tracking type.

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